REMARKS

Claims 52, 54-73, and 75-122 are pending. Claims 52, 72, 80 and 81 have been amended. Claim 53 and 74 have been canceled. Claims 82-122 are new.

A clean copy of the pending claims is attached for the Examiner's convenience.

I. Section 112 Rejections:

This problem noticed by the Examiner has been fixed by adding antecedent basis for the "clock signal" in the preamble of independent claim 72.

II. Obviousness-Type Double Patenting Rejection:

All of the claims have been rejected for obviousness-type double patenting in light of certain claims in USP 6,680,874. A Terminal Disclaimed is filed herewith to obviate this basis for rejection.

III. Art-Based Rejections:

Claims 52, 55, 58, 72, 73, 80, and 81 have been rejected as anticipated under 35 U.S.C. § 102(b) by USP 5,939,913 ("Tomita").

Applicant has rendered all of its independent claims (including the new independent claims) allowable by incorporating certain limitations from dependent claims that have not been rejected on the basis of Tomita. Specifically:

- Claim 52 has been amended to incorporate the limitations of claim 53.
- Claim 72 has been amended to incorporate the limitations of claim 74.
- Claims 80 and 81 have been amended to incorporate the limitations of claim 79.
- New independent claim 82 comprises previous claim 56 written in independent form.
- New independent claim 92 comprises previous claim 60 written in independent form.

- New independent claim 102 comprises previous claim 76 written in independent form.
- New independent claim 109 comprises previous claim 78 written in independent form.
- New independent claim 116 comprises previous claim 79 written in independent form.

In short, all of Applicant's independent claims (and by necessity associated dependent claims) are believed patentable in light of Tomita.

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Applicant believes pending claims 52, 54-73, and 75-122 to be patentable, and requests that a Notice of Allowance issue for these claims.

Should the Examiner have any question regarding this submission, please contact the undersigned.

Respectfully submitted,

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52. (previously added; currently amended) A method of synchronizing a clock signal using a delay lock loop, comprising:

initially fixing a control signal to a reset value;

frequency dividing the clock signal to provide a divided signal;

coupling the divided signal to an input of a variable delay circuit, the variable delay circuit outputting a delayed signal;

comparing the divided signal to a phase of the delayed signal to modify the initially fixed control signal; and

applying the modified control signal to the variable delay circuit to control its delay.

53. (canceled)

54. (previously added) The method of claim 53, wherein the reset value sets the variable delay circuit to a minimum setting.

55. (previously added) The method of claim 52, wherein the variable delay circuit includes a propagation delay.

56. (previously added) The method of claim 52, wherein the control signal comprises use of an integrator.

57. (previously added) The method of claim 52, wherein the control signal comprises use of a charge pump.

58. (previously added) The method of claim 52, wherein comparing the divided signal to a phase of the delayed signal to generate a control signal involves assessing the phase difference between the divided signal and the delayed signal.

59. (previously added) The method of claim 52, wherein the method produces the delayed signal such that it is synchronized with reading or writing of data to and from a memory array.

60. (previously added) The method of claim 59, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

61. (previously added) The method of claim 60, further comprising selecting one of the delayed representations to synchronize the reading and writing.

62. (previously added) The method of claim 61, wherein selecting is accomplished by a multiplexer.

63. (previously added) A method of locking a delay lock loop in synchronization with a clock signal, comprising:

initializing a variable delay circuit within the delay lock loop to a minimum delay value, wherein the output of the variable delay circuit is coupled to a feedback loop, and wherein delay of the variable delay circuit is controlled by a control signal generated by the feedback loop;

frequency dividing the clock signal and inputting it into the variable delay circuit; and

locking the frequency-divided clock signal by adjusting the control signal to the variable delay circuit.

64. (previously added) The method of claim 63, further comprising coupling a frequency divider into the feedback loop after locking.

65. (previously added) The method of claim 63, wherein the variable delay circuit includes a propagation delay.

66. (previously added) The method of claim 63, wherein the feedback loop comprises a phase detector for comparing the phase difference between the clock signal and the output of the variable delay circuit.

67. (previously added) The method of claim 66, further comprising an integrator coupled to the phase detector for producing the control signal.

68. (previously added) The method of claim 63, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

69. (previously added) The method of claim 68, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

70. (previously added) The method of claim 69, further comprising selecting one of the delayed representations to synchronize the reading and writing.

71. (previously added) The method of claim 70, wherein selecting is accomplished by a multiplexer.

72. (previously added; currently amended) A delay lock loop circuit for processing a control signal, comprising:

a variable delay circuit configured to receive a frequency divided version of the clock signal;

a phase detector for receiving as inputs (i) the output of the variable delay circuit and (ii) the frequency divided version of the clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

73. (previously added) The circuit of claim 72, wherein the variable delay circuit includes a propagation delay.

74. (canceled)

75. (previously added) The circuit of claim 72, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

76. (previously added) The circuit of claim 75, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the output of the variable delay circuit.

77. (previously added) The circuit of claim 76, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

78. (previously added) The circuit of claim 72, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

79. (previously added) The circuit of claim 72, wherein the control signal is resettable to a minimum value.

80. (previously added; currently amended) A memory device accessible by a first clock signal, comprising:

a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal, and (ii) the frequency divided version of the first clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit, and wherein the control signal is resettable to a minimum value.

81. (previously added; currently amended) A system, comprising:

a microprocessor for producing a first clock signal;

a memory device for receiving the first clock signal, the memory device comprising a memory array accessible by a second clock signal; and

a delay lock loop for synchronizing the second clock signal with the first clock signal, comprising:

a variable delay circuit for producing the second clock signal, wherein the variable delay circuit is configured to receive a frequency divided version of the first clock signal;

a phase detector for receiving as inputs (i) either the second clock signal, and (ii) the frequency divided version of the first clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal;

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit, and wherein the control signal is resettable to a minimum value.

82. (new) A method of synchronizing a clock signal using a delay lock loop, comprising:

frequency dividing the clock signal to provide a divided signal;

coupling the divided signal to an input of a variable delay circuit, the variable delay circuit outputting a delayed signal;

comparing the divided signal to a phase of the delayed signal to generate a control signal, wherein the control signal comprises use of an integrator; and

applying the control signal to the variable delay circuit to control its delay.

83. (new) The method of claim 82, further comprising initially fixing said control signal to a reset value.

84. (new) The method of claim 83, wherein the reset value sets the variable delay circuit to a minimum setting.

85. (new) The method of claim 82, wherein the variable delay circuit includes a propagation delay.

86. (new) The method of claim 82, wherein the control signal comprises use of a charge pump.

87. (new) The method of claim 82, wherein comparing the divided signal to a phase of the delayed signal to generate a control signal involves assessing the phase difference between the divided signal and the delayed signal.

88. (new) The method of claim 82, wherein the method produces the delayed signal such that it is synchronized with reading or writing of data to and from a memory array.

89. (new) The method of claim 88, further comprising coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal.

90. (new) The method of claim 89, further comprising selecting one of the delayed representations to synchronize the reading and writing.

91. (new) The method of claim 90, wherein selecting is accomplished by a multiplexer.

92. (new) A method of synchronizing a clock signal using a delay lock loop, comprising:

frequency dividing the clock signal to provide a divided signal;

coupling divided signal to an input of a variable delay circuit, the variable delay circuit outputting a delayed signal;

coupling the delayed signal to a vernier circuit to produce various delayed representations of the delayed signal;

comparing the divided signal to a phase of the delayed signal to generate a control signal; and

applying the control signal to the variable delay circuit to control its delay.

93. (new) The method of claim 92, further comprising initially fixing said control signal to a reset value.

94. (new) The method of claim 93, wherein the reset value sets the variable delay circuit to a minimum setting.

95. (new) The method of claim 92, wherein the variable delay circuit includes a propagation delay.

96. (new) The method of claim 92, wherein the control signal comprises use of an integrator.

97. (new) The method of claim 92, wherein the control signal comprises use of a charge pump.

98. (new) The method of claim 92, wherein comparing the divided signal to a phase of the delayed signal to generate a control signal involves assessing the phase difference between the divided signal and the delayed signal.

99. (new) The method of claim 92, wherein the method produces the delayed signal such that it is synchronized with reading or writing of data to and from a memory array.

100. (new) The method of claim 99, further comprising selecting one of the delayed representations to synchronize the reading and writing.

101. (new) The method of claim 100, wherein selecting is accomplished by a multiplexer.

102. (new) A delay lock loop circuit for processing a control signal, comprising:

a variable delay circuit configured to receive a frequency divided version of the clock signal;

a vernier circuit coupled for producing various delayed representations of the output of the variable delay circuit;

a phase detector for receiving as inputs (i) the output of the variable delay circuit and (ii) the frequency divided version of the clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal,

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit.

103. (new) The circuit of claim 102, wherein the variable delay circuit includes a propagation delay.

104. (new) The circuit of claim 102, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

105. (new) The circuit of claim 102, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

106. (new) The circuit of claim 102, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

107. (new) The circuit of claim 102, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.

108. (new) The circuit of claim 102, wherein the control signal is resettable to a minimum value.

109. (new) A delay lock loop circuit for processing a control signal, comprising:

a variable delay circuit configured to receive a frequency divided version of the clock signal;

a phase detector for receiving as inputs (i) the output of the variable delay circuit and (ii) the frequency divided version of the clock signal, and for producing a first signal indicative of the phase difference between the two phase detector inputs;

a feedback loop for receiving the first signal and for producing a control signal; and

a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal,

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit when not interrupted by the lock sequencer circuit.

110. (new) The circuit of claim 109, wherein the variable delay circuit includes a propagation delay.

111. (new) The circuit of claim 109, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

112. (new) The circuit of claim 109, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

113. (new) The circuit of claim 112, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the output of the variable delay circuit.

114. (new) The circuit of claim 113, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

115. (new) The circuit of claim 109, wherein the control signal is resettable to a minimum value.

116. (new) A delay lock loop circuit for processing a control signal, comprising:

a variable delay circuit configured to receive a frequency divided version of the clock signal;

a phase detector for receiving as inputs (i) the output of the variable delay circuit and (ii) the frequency divided version of the clock signal, and for

producing a first signal indicative of the phase difference between the two phase detector inputs; and

a feedback loop for receiving the first signal and for producing a control signal,

wherein the control signal is received by the variable delay circuit to adjust the delay of the variable delay circuit, and wherein the control signal is resettable to a minimum value.

117. (new) The circuit of claim 116, wherein the variable delay circuit includes a propagation delay.

118. (new) The circuit of claim 116, wherein the feedback loop comprises an integrator coupled to the first signal for producing the control signal.

119. (new) The circuit of claim 116, wherein the output of the variable delay circuit is synchronized with reading or writing of data to and from a memory array.

120. (new) The circuit of claim 119, further comprising a vernier circuit coupled between the variable delay circuit and the phase detector for producing various delayed representations of the output of the variable delay circuit.

121. (new) The circuit of claim 120, further comprising a multiplexer for selecting one of the delayed representations to synchronize the reading and writing.

122. (new) The circuit of claim 116, further comprising a lock sequencer circuit, wherein the lock sequencer circuit can interrupt the control signal.